Doc Code: AP.PRE.REQ

PTO/SB/33 (07-05)
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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
915-008.012

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on May 29, 2007

Signature Kathleen Sipos

Typed or printed name Kathleen Sipos

Application Number 10/634,734	Filed August 4, 2003
First Named Inventor Antti KIIVERI et al.	
Art Unit 2132	Examiner V. Perungavoor

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

□ applicant/inventor.

□ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

□ attorney or agent of record.
Registration number ____________.

☒ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 58,051

Signature

Keith R. Obert
Typed or printed name

203-261-1234
Telephone number

May 29, 2007
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☒ *Total of 2 forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Attorney Docket No. 915-008.012
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re Application of :

Antti KIIVERI et al : Confirmation No. **6648**

Serial No. **10/634,734** : Examiner: **V. Perungavoor**

Filed: **August 4, 2003** : Group Art Unit: **2132**

For: **SECURE EXECUTION ARCHITECTURE**

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Sir:

This Pre-Appeal Brief Request for Review is submitted in response to the final Office Action of February 27, 2007.

CERTIFICATE OF MAILING

I hereby certify that this communication is being deposited with the United States Postal Service today, May 29, 2007, in an envelope with sufficient postage as first-class mail addressed to: Mail Stop AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Kathleen Sipos

Kathleen Sipos

REMARKS

Claims 1-18 were examined by the Office, and all claims are rejected. Applicant respectfully requests review and withdrawal of the rejections because the Office has committed clear error in rejecting the claims. The Office has committed clear error by failing to show that each and every limitation recited in the claims is disclosed or suggested by the cited references.

This Request for Review is submitted along with a Notice of Appeal.

Claim Rejections Under § 102

On page 2 of the Office Action, claims 1-4, 6-10 and 12 are rejected under 35 U.S.C. § 102(e) as anticipated by Moscovici et al. (U.S. Patent No. 6,678,765). Applicant respectfully submits that the Office has committed clear error in rejecting claim 1, because the Office fails to show that Moscovici discloses or suggests each and every limitation recited in claim 1. Moscovici at least fails to disclose or suggest setting a processor in one of at least two different operating modes, in the first operating mode the processor is able to access a storage area in which protected data related to circuitry security is located, and in the second operating mode the processor is prevented from accessing the storage area, as recited in claim 1. In addition, Moscovici also fails to disclose or suggest the storage area in which protected data relating to circuitry security is located, as recited in claim 1.

The present invention, as defined by the independent claims, is based on the idea that circuitry is provided in which a processor is operable in at least two different modes, a first secure operating mode and a second unsecure operating mode. In the first secure operating mode, the processor has access to security related data located in various memories located within the circuitry. The security data include cryptographical keys and algorithms, software for booting the circuitry, secret data such as random numbers used as cryptographical key material, application programs etc. The access to these security data and the processing of them need to be restricted, since an intruder with access to security data could manipulate a device, for example a mobile terminal, in which the circuitry of the present invention is implemented. The present invention advantageously enables the processor of the circuitry to execute non-verified software downloaded into the circuitry when the second processor operating mode is set.

In contrast to the present invention, Moscovici relates to an embedded modem that has two processors, a general purpose processor (CPU) for executing lengthy programs, and a digital signal processor (DSP) for executing short programs. See Moscovici column 1, lines 5-8. The Office asserts on page 2 of the final Office Action of February 27, 2007 that the external memory module (34) of Moscovici contains data related to the handshaking process, and this data relates to a security feature of the circuitry. However, Moscovici actually discloses that during the handshake process various parts of the modem are configured and various parameters that effect the transmission of data over the communication link are set. See Moscovici column 1, lines 18-21. Moscovici discusses a four phase handshaking process in which during phase 1 the modems exchange signals that allow the modems to determine some negotiation parameters such as which recommendations are supported by the modems and which modulation modes are available. The other phases generally involve other setup parameters and characteristics such as symbol rate, power level, and training. See Moscovici column 1, lines 26-55. Contrary to the assertions of the Office, Moscovici never mentions that security information related to the modems is exchanged or accessed during the handshaking process. Instead, the modem handshaking process is merely to enable communication between the modems and has nothing to do with security of the modems. Furthermore, the Office also asserts that the operating system usually has protected data and is only accessible by the CPU during control operations. However, Moscovici does not disclose or suggest that the operating system has protected data, and in fact states that the memory module stores CPU <u>control</u> programs, such as an operating system that enables the CPU to perform various tasks. See Moscovici column 3, lines 40-42. Therefore, the operating system is not protected data that relates to circuitry security, but instead is only for controlling the operations of the CPU. In addition, the CPU must be able to access, or at least receive control information from the operating system at all times in order to allow control of the CPU. Therefore, for at least this reason Moscovici fails to disclose or suggest a storage area in which protected data relating to circuitry security is located, as recited in claim 1.

Furthermore, Moscovici also fails to disclose or suggest setting a processor in one of at least two different operating modes, in the first operating mode the processor is able to access a storage area in which protected data related to circuitry security is located, and in the second operating mode the processor is prevented from accessing the storage area, as recited in claim 1. The Office asserts that the CPU and DSP use the memory module and buffers to fetch and execute instructions alternatively, and therefore since only one CPU or DSP can access the module and registers, access by the other one is effectively prevented. However, Moscovici does not disclose or suggest that only one of the CPU or DSP can access the memory module or buffers at any given time. In fact, Moscovici discloses that the CPU writes a set of instructions to the external memory module that indicate which DSP programs are to be executed by the DSP, and then notifies the DSP that the instructions are present in the instruction buffer. See Moscovici column 4, line 66—column 5, line 3. Moscovici does not disclose that only one of the CPU or DSP may access the instruction buffer at a given time, and therefore does not disclose or suggest that access is prevented by either the CPU or DSP when the other one is accessing the instruction buffer. In addition, even assuming that access is prevented, which applicant does not admit, the Office previously asserted that the protected data relating to circuitry security was the operating system located in the internal memory module (34). There is no mention that the CPU or the DSP alternatively access the internal memory module (34), and Moscovici in fact discloses that the memory module stores a plurality of DSP programs that enable the DSP to perform various tasks. See Moscovici column 3, lines 47-48. Therefore, the external memory module (37) with instruction buffer does not have the operating system or programs that control the DSP, and it is irrelevant whether the CPU and DSP alternatively access the external memory module (37) because it does not contain the programs that the Office asserts corresponds to the protected data relating to circuitry security.

The Office has committed clear error in rejecting claim 1, because the Office incorrectly takes disparate teachings of Moscovici to arrive at the limitations recited in claim 1. In order to anticipate a claim, the elements must be arranged as required by the claim. See MPEP § 2131. Claim 1 requires a storage area with protected data relating to circuitry security, and a processor that may access the storage area when a first processor operating mode is set, and the processor is prevented from accessing the storage area when a second processor operating mode is set. Moscovici does not disclose or suggest that either the CPU or DSP are ever prevented from accessing the internal memory module (37). Therefore, for at least the reasons discussed above, Moscovici fails to disclose or suggest all of the limitations recited in claim 1, and the Office has committed clear error in rejecting claim 1.

Independent claims 7 and 13 contain limitations similar to those recited in claim 1, and are rejected for the same reasons as claim 1. Therefore, for at least the reasons discussed above in relation to claim 1, claims 7 and 13 are not disclosed or suggested by Moscovici.

The claims depending from the above mentioned independent claims are not disclosed or suggested by Moscovici at least in view of their dependencies.

Claim Rejections Under § 103

Regarding the obviousness rejection of dependent claims 5, 11 and 17, Smith (U.S. Patent No. 6,449,281) does not add any substantial matter that can compensate for the lacking features of Moscivici, and therefore the claims rejected on this ground are patentable at least in view of their dependencies.

Conclusion

It is respectfully submitted that the present application is in condition for allowance, and such action is earnestly solicited. The undersigned hereby authorizes the Commissioner to charge Deposit Account No. 23-0442 for any fee deficiency required to submit this response.

Respectfully submitted,

Date: 29 May 2007

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